REMARKS

Claims

Claims 2-9, and 11-14 are pending in this application. Claims 1, 10 and 15 have been canceled without prejudice or disclaimer. Claims 2-4, 9 and 11-14 have been amended. No new matter has been added.

Claim Rejections under 35 USC § 103

Claims 1, 10 and 15 are rejected under 35 USC § 103(a) as being unpatentable over the IBM publication, *IBM TotalStorage Enterprise Storage Server Model 800*, (hereafter "IBM") in view of U.S. Patent No. 5,123,099 issued to Shibata et al. (Shibata), further in view of Kinjo et al., U.S. Patent 6,944,684. The rejection should be withdrawn I view of the cancellation of these claims without prejudice or disclaimer.

Claims 2-7 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over IBM, Shibata et al. and Kinjo et al. as applied to claims 1, 10 and 15 above, and further in view of Beardsley et al., U.S. Patent No. 5,437,022 (hereafter Beardsley). Claims 8 and 14 are rejected under 35 U.S.C. §103(a) as being unpatentable over IBM, Shibata et al., Kinjo et al. and Beardsley et al. as applied to claims 1-7, 10-13 and 15 above, and further in view of Yanai et al., U.S. Patent Publication Number 2003/0005355. Claim 9 is rejected under 35 U.S.C. §103(a) as being unpatentable over Shibata et al., IBM, Kinjo et al., in view of Matsumoto et al., U.S. Patent No. 5,720,028. Applicants request reconsideration of these rejections for the following reasons.

With respect to claim 2, the Examiner relies upon the combination of IBM, Shibata and Kinjo to teach the features of claim 2, except for the power system. Beardsley is relied upon for teaching the power system.

In particular, Beardsley is relied upon for disclosing a first power unit and a second power unit (80, 90 in Fig. 4). The first memory (CACHE A in Fig. 4) of the first controller receives power from the first power unit and the second memory NVS A (of the first controller) and the third memory (cache B) of the second controller receives power from the second power unit. Whereas the claimed first controller and second controller arguably correspond to the respective cages 0 and 1 in Figure 4 of Beardsley, the NVS A in cage 1 does not correspond to the second memory of the first controller as asserted in the Office Action because the first controller corresponds to cage 0. In order for NVS A in cage 1 to be the second memory of the first controller and also cache B to be the third memory of the second controller, the distinction between the first and second controllers in the present invention would not be maintained and, as a result, the second and third memory would be included in the same controller in cage 1.

In the present invention, the first controller transfers data stored in the second memory of the first controller to the third memory of the second controller. In contrast, Beardsley discloses that NVS A (60) or NVS B (59) are invoked to destage write data to a DASD respectively when cache A or cache B fails (see fig. 5, tables 1 and 2 and column 7, lines 48-60), however Beardsley does not disclose storing data that is stored at NVS A or B directly in cache A or B. Accordingly, the second memory of the first controller according to the present invention functions differently from NVS A or B of Beardsley, and therefore the reference does not disclose the power system claimed by Applicants.

According to the present invention, the second memory of the first controller is capable of speeding up data writing, thereby achieving improved performance which is one of the main objects of the present invention. The second memory of the first controller and the first memory of the first controller receive power from different power units, mainly the second power unit and the first power unit. As a result, even if the first power unit applying power to the first memory of the first controller fails, the second memory of the first controller can receive normal power from the second power unit, and it is possible to achieve the main effect of speeding up of data writing, along with securing the power supply upon failure. If NVS A in cage 1 of Beardsley is used as a second memory of the first controller, as suggested in the Office Action, data writing will be slow because NVSA is not incorporated in the first controller, i.e. cage 0. In addition, since the system discloses by Beardsley does not include any subsequent operation of transferring the data stored in NVS A to cache A or cache B, the amount of data that can be written is limited to the capacity of NVS A.

In claim 3, the combination of IBM, Shibata and Kinjo and Beardsley is used to reject the claim. Beardsley is applied to show a first memory that receives power from a first power unit, a second memory from a second power unit, and a third memory from a third power unit, respectively. However, as forementioned, the second memory according to the present invention and NVS A or B of Beardsley are different and do not correspond to each other. Further, the DC power supplies 92 and 96 are connected to the same AC power supply 90 in Beardsley, and the DC supplies 92, 94 and 96 function as a power unit as a result of being combined with the AC power supply 90. On the other hand, the power units of claim 3 are claimed to be first, second and third power units, respectively. Since the DC power supply 92

and 96 are connected to the same AC power supply 90 in Beardsley, if a single failure occurs in the AC power supply 90, both DC power supply 92 and 96 will fail as well. Therefore, the power supplies disclosed by Beardsley are not equivalent, according to one having ordinary skill in the art, to the first, second and third power unit as claimed by Applicants, in which if there were a single failure among the claimed power units, the other of the power units would not fail as well.

Claim 4 has been rejected by relying on the combination of IBM, Shibata, Kinjo and Beardsley, and in particular on IBM for teaching a battery with a second memory (page 89 of the reference). The reference is also been relied upon for teaching a battery charging system on page 30 of the reference. However, Applicants point out that IBM teaches the existence of a battery that powers the NVS (page 89). As shown in Figure 3-2 on page 51, the NVSs mutually store write-data of another cluster (another controller) while the second memory of the first controller according to the present invention stores write-data of the first controller, and thus the elements are not comparable. Further, while in the present invention, the data stored in the second memory of the first controller is then written to the third memory of the second controller, IBM does not disclose this aspect of the invention. Should the second memory of the first controller, according to the present invention, be interpreted as corresponding to the NVS disclosed by IBM, the main effect of the invention, i.e. the speeding up of data-write is not achievable. The main effect of the invention is achieved by storing data in the second memory which is incorporated in the same controller as that of the first memory prior to the storing of data in another controller. This combination is different from that disclosed in the IBM reference, therefore the reference does not show the invention as claimed.

Beardsley is also applied along with IBM, Shibata and Kinjo in the rejection of claim 11. Specifically, Beardsley is relied upon for teaching a third cache memory for being connected to the second power unit (61, 92 in Figure 4). Further, according to the Office Action, Shibata is relied upon for teaching that the third memory can be a FIFO buffer. In particular, the Office Action cites column 4, lines 39-44 for teaching that the third memory can be a FIFO buffer. However, Shibata merely states that the is that data being written to a FIFO memories 25 and 25'n are connected in parallel with the cache memories. One having ordinary skill in the art would not combine the teachings of Shibata with Beardsley. According to claim 11, by supplying power to the FIFO buffer, which is capable of high speed data-write via a power unit different from that of the first cache memory, data-write can be achieved at high speed and the supply of power can be maintained.

With respect to claim 12, the combination of IBM, Shibata and Kinjo is relied upon in the rejection in combination with Beardsley. Beardsley is relied upon for teaching a third cache memory that is connected to second and third power units. Shibata is relied upon for teaching a third memory that can be a FIFO buffer. However, as mentioned with respect to the rejection of claim 11, the disclosure of Shibata does not disclose a third power unit connected to a FIFO buffer. In addition, Beardsley does not disclose the first through third power units, wherein the power units are independent, as claimed by Applicants in claim 12.

With respect to claim 13, the claim is patentable over the references relied upon in the rejection for the same reasons as claims 11 and 12 are patentable over these references.

Independent claim 9 has been rejected using Matsumoto in combination with IBM, Shibata and Kinjo. Matsumoto is relied upon for teaching a switching unit. However, as shown

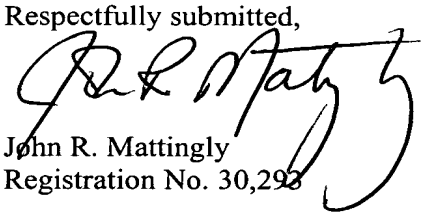
in Figure 2 of Matsumoto, the switching unit 220 is an element of the controller 200 and functions to switch reception of the request to and from host I-F controllers 210 and 410 from a host computer (Fig. 6). On the other hand, the switching unit recited in claim 9 is an element independent from the first and second controllers, and connects the host interface unit with the first and second controllers. Accordingly, the claimed switching unit of Figure 9 is not suggested by the switching unit 220 and Matsumoto. Accordingly, the rejection of claim should be withdrawn.

The remainder of the pending claims are dependent claims and set forth additional limitations that are not disclosed or suggested by the art of record. Accordingly each of these claims should be allowed at least for depending from an allowable base claim and further for being patentable over the art of record.

Conclusion

In view of the foregoing amendments and remarks, Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,



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